WHAT IS CLAIMED IS:

1. A computer device comprising:

a CPU for outputting an address signal and also outputting an access signal twice for the same address signal;

a memory for storing a series of programs, the memory receiving the address signal and the access signal from the CPU and outputting a program located at an address corresponding to the address signal twice in response to the access signal;

a latch circuit for latching the program output from the memory, according to the access signal; and

a match detection circuit for comparing the two programs at the same address output from the memory, that is, a first-time program output from the latch circuit and a second-time program output from the memory, and detecting matching of the two programs,

wherein the CPU receives a comparison result signal from the match detection circuit, and outputs the access signal for the same address again if the matching of the programs fails, so that the match detection circuit performs comparison of a third-time program output from the memory with the second-time program output from the latch circuit.

2. The computer device of Claim 1, wherein the first-time, second-time, and third-time programs are output from

the memory in an instruction fetch cycle, and

when the match detection circuit detects matching between the second-time program and the third-time program, the CPU proceeds to a decode cycle for the matching program.

3. A computer device comprising:

a CPU for outputting an address signal and also outputting an access signal three times or more for the same address signal;

a memory for storing a series of programs and outputting a program located at an address corresponding to the address signal sequentially in response to the access signal output three times or more;

a plurality of latch circuits connected in series for latching the program output from the memory sequentially in response to the access signal output three times or more; and

a match detection circuit for comparing the plurality of programs at the same address output from the memory, that is, a program output last from the memory and programs output from the respective latch circuits, and detecting matching of all the programs,

wherein when the match detection circuit detects matching of all the programs, the CPU proceeds to a decode cycle for the matching program.

4. The computer device of Claim 3, wherein a majority circuit for determining a program based on majority rule among the plurality of programs at the same address output from the memory is provided in place of the plurality of latch circuits and the match detection circuit, and

the CPU decodes the program determined as the majority by the majority circuit.

5. A computer device comprising:

a memory for storing a series of programs; and

a CPU for sequentially fetching programs from the memory in a pipeline, and decoding and executing the programs,

wherein the CPU fetches a first program from the memory in a fetch cycle,

in a decode cycle for the first program, the CPU fetches a second program succeeding to the first program, and also requests the memory to re-read the first program, compares the re-read first program with the first program fetched in the fetch cycle for the first program, and proceeds to execution of the first program if the two programs match with each other.

6. The computer device of Claim 5, wherein if the two programs fail to match with each other, the CPU requests the memory to second re-read the first program, compares the sec-

ond re-read first program with the re-read first program, and proceeds to execution of the first program if the two programs match with each other.

7. The computer device of Claim 5, wherein the memory receives an address signal from the CPU, and outputs a program located at an address corresponding to the address signal and a program at an address immediately preceding the address corresponding to the address signal.

8. The computer device of Claim 7, wherein the memory stores a series of programs in rows and columns in the address order, and

on receipt of the address signal from the CPU, the memory outputs two continuous row selection signals and two continuous column selection signals.

9. The computer device of Claim 6, further comprising a latch circuit,

wherein the latch circuit latches the first program output from the memory in the fetch cycle in synchronization with the access signal output from the CPU, and

a match detection circuit is connected to the CPU for detecting matching between the first program latched by the latch circuit and the first program re-read in the decode cy-

cle.

10. The computer device of Claim 9, wherein when the first program is re-read in the decode cycle, the latch circuit latches the re-read first program, and the match detection circuit detects matching between the second re-read first program read when the two first programs fail to match with each other and the re-read first program latched by the latch circuit.

Report Method